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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/611,910	07/03/2003	Atsushi Fujisawa	501.36384CC9	5578

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EXAMINER	
CAO, PHAT X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 04/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/611,910	FUJISAWA ET AL.	
	Examiner	Art Unit	
	Phat X. Cao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-7 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-7 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/126,438.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7/3/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1, 6 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Glenn (US. 6,150,193).

Glenn (Figs. 1 and 7C) discloses a method of manufacturing a semiconductor package, comprising: (a) providing a plurality of semiconductor chips 30 and a wiring substrate 12, each of the plurality of semiconductor chips 30 having an integrated circuit and bonding pads formed on a main surface thereof, the wiring substrate 12 having a

first surface, a second surface opposed to the first surface and a plurality of conductive layers 22, the wiring substrate 12 having a plurality of chip mounting areas at the first surface in a plane view, the plurality of chip mounting areas being arranged in a matrix formation (Fig. 7C); (b) mounting the plurality of semiconductor chips 30 on the plurality of chip mounting areas of the first surface of the wiring substrate 12 respectively; (c) electrically connecting the bonding pads of the semiconductor chips 30 with corresponding conductive layers 22 of the plurality of conductive layers, by a plurality of bonding wires 40; (d) sealing the plurality of semiconductor chips 30, the plurality of bonding wires 40 and the first surface of the wiring substrate 12 including the plurality of chip mounting areas by a resin member 42; (e) forming a plurality of bump electrodes 28 on the second surface of the wiring substrate 12 so as to electrically connect with the plurality of conductive layers 22 of the wiring substrate 12; and (f) after (e) dividing the wiring substrate 12 into plural parts each including a corresponding chip mounting area of the plurality of chip mounting area, thereby to form a plurality of semiconductor packages 10 each including one of the plural parts of the wiring substrate 12, one of the plurality of semiconductor chips 30, one of the plurality of bonding wires 40 and a part of the resin member 42 (see column 11, lines 38-44); wherein mounting in step (b) includes fixing each of the plurality of semiconductor chips 30 on the first surface of the wiring substrate 12 by an insulating adhesive layer 34 respectively.

4. Claims 1 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee et al (US. 6,054,338).

Lee (Figs. 3, 4 and 10) discloses a method of manufacturing a semiconductor

package 20, comprising: (a) providing a plurality of semiconductor chips 28 having an integrated circuit and a wiring substrate 24, each of the plurality of semiconductor chips 28 having an integrated circuit and bonding pads formed on a main surface thereof, the wiring substrate 24 having a first surface, a second surface opposed to the first surface and a plurality of conductive layers 92 (Fig. 10), the wiring substrate 24 having a plurality of chip mounting areas being arranged in a matrix formation (Fig. 3); (b) mounting the plurality of semiconductor chips 28 on the plurality of chip mounting areas of the first surface of the wiring substrate 24 respectively; (c) electrically connecting the bonding pads of the semiconductor chips 28 with corresponding conductive layers 92 of the plurality of conductive layers, by a plurality of bonding wires 29; (d) sealing the plurality of semiconductor chips 28, the plurality of bonding wires 29 and the first surface of the wiring substrate 24 including the plurality of chip mounting areas by a resin member 32; (e) forming a plurality of bump electrodes 30 (Fig. 4) or 106 (Fig. 10) on the second surface of the wiring substrate so as to electrically connect with the plurality of conductive layers 92 of the wiring substrate; and (f) after step (e), dividing the wiring substrate 24 into plural parts each including a corresponding chip mounting area of the plurality of chip mounting areas, thereby to form a plurality of semiconductor packages 20 each including one of the plurality of semiconductor chips 28, one of the plurality of bonding wires 29 and a part of the resin member 32 (Fig. 4).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Glenn **or** Lee et al in view of Mullen, III et al (US. 5,241,133).

Regarding claims 2-3, neither Glenn nor Lee discloses the wiring substrate is a flexible tape substrate of polyimide.

However, Mullen (Fig. 4) teaches the forming of a semiconductor package having a semiconductor chip 24 formed on a wiring flexible tape substrate 22 of polyimide (column 3, lines 5-21). Accordingly, it would have been obvious to form the wiring substrate of either Glenn **or** Lee with a flexible tape substrate of polyimide because as taught by Mullen, such wiring substrate would provide a flexible circuitry (column 3, lines 9-13).

Regarding claims 4-5, Glenn (Fig. 1) **or** Lee (Fig. 10) further discloses the wiring substrate includes a plurality of through holes passing through the wiring substrate in a thickness direction, wherein portions of the plurality of conductive layers 22 of Glenn or 92 of Lee are arranged to cover the plurality of through holes at the first surface of the wiring substrate, and wherein the plurality of solder bump electrode 28 of Glenn or 106 of Lee are formed at the plurality of through holes so as to contact with the portions of the plurality of conductive layers.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is (571) 272-1703. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PHAT X. CAO
PRIMARY EXAMINER

PC
April 2, 2004